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| 10/709,048 | 04/08/2004 | Sadanand V. Deshpande | FIS920030397US1 | 3047 |

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FREDERICK W. GIBB, III
Gibb & Rahman, LLC
2568-A RIVA ROAD
SUITE 304
ANNAPOLIS, MD 21401

| EXAMINER | |
|---|---|
| INGHAM, JOHN C | |
| ART UNIT | PAPER NUMBER |
| 2814 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/709,048 | DESHPANDE ET AL. | |
| | Examiner | Art Unit | |
| | John C. Ingham | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,2,4-9,12-14 and 26-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9,12-14 and 26-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

**DETAILED ACTION**

1. The amendments filed 26 June 2007 have been entered.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **1-2, 4-9 and 12-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Luning (US 6,506,642) and Nandakumar (US 6,479,339).

4. Regarding claims **1-2, 4-9 and 12-14**, Luning discloses in Figure 6 an integrated circuit structure comprising: a substrate (40); first-type transistors (left side nFET) on said substrate, wherein said first-type transistors comprise first gate conductors (41) and first spacers (60) adjacent said first gate conductors; second-type transistors (right side pFET) on said substrate, wherein said second-type transistors comprise second gate conductors (42), said first spacers (44) adjacent said second gate conductors, said first spacers adjacent said second gate conductors and second spacers (60); first-type (N type) source/drain impurity implants (61) in areas of said substrate completely outside of and adjacent to said first spacers of said first gate conductors; second-type (P type) source/drain impurity implants (62) in areas of said substrate completely outside of and adjacent to said second spacers of said second gate conductors,

wherein said first type impurity is spaced closer to said first gate conductors than said second type impurity is spaced from said second gate conductors; first silicide regions (64) proximate said first spacers of first-type transistors; and second silicide regions (63) proximate said second spacers of said second-type transistors, wherein said second silicide regions are farther from said second gate conductors than said first silicide regions are from said first gate conductors (W3 greater than W2).

Luning does not disclose an etch stop layer on said first spacers of the second-type transistor, and second spacers on said etch stop layer, wherein said etch stop layer is only on said first spacers that are adjacent said second gate conductors and said etch stop layer is not on said first spacers that are adjacent said first gate conductors; wherein said second spacers are only on said etch stop layer on said first spacers that are adjacent said second gate conductors, and said second spacers are not adjacent said first spacers that are adjacent said first gate conductors. Instead Luning shows that the double spacer is only on the second-type transistor, with no etch stop layer between the double spacer.

Nandakumar teaches in Fig 3C that a nitride etch stop layer (270) is formed on one transistor (right side of Fig), between spacer layers of oxide (130, 280) , in order to allow selective etching (col 5 ln 21-23) and results in no additional masking steps (col 2 ln 6-10). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the etch stop of Nandakumar on the device of Luning in order to form mixed voltage circuits without the need for additional masking steps.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims **26-34** are rejected under 35 U.S.C. 103(a) as being unpatentable over Luning and Fulford (US 6,258,680).

8. Regarding claims **26-29**, Luning discloses in Figure 6 an integrated circuit structure comprising: a substrate (40); first-type transistors (left side nFET) on said substrate, wherein said first-type transistors comprise first gate conductors (41) and first spacers (60) adjacent said first gate conductors; second-type transistors (right side pFET) on said substrate, wherein said second-type transistors comprise second gate conductors (42), said first spacers (44) adjacent said second gate conductors, said first spacers adjacent said second gate conductors and second spacers (60); first-type (N

type) source/drain impurity implants (61) in areas of said substrate completely outside of and adjacent to said first spacers of said first gate conductors; second-type (P type) source/drain impurity implants (62) in areas of said substrate completely outside of and adjacent to said second spacers of said second gate conductors, wherein said first type impurity is spaced closer to said first gate conductors than said second type impurity is spaced from said second gate conductors; first silicide regions (64) proximate said first spacers of first-type transistors; and second silicide regions (63) proximate said second spacers of said second-type transistors, wherein said second silicide regions are farther from said second gate conductors than said first silicide regions are from said first gate conductors (W3 greater than W2).

Luning does not disclose an oxide layer on said first gate conductors and said second gate conductors, wherein said first spacers are on said oxide layer, or an etch stop layer on said first spacers of the second-type transistor, and second spacers on said etch stop layer, wherein said etch stop layer is only on said first spacers that are adjacent said second gate conductors and said etch stop layer is not on said first spacers that are adjacent said first gate conductors; wherein said second spacers are only on said etch stop layer on said first spacers that are adjacent said second gate conductors, and said second spacers are not adjacent said first spacers that are adjacent said first gate conductors. Instead Luning shows that a double spacer (of nitride) is only on the second-type transistor, with no etch stop layer between the double spacer.

Fulford teaches in Fig 12 that an oxide liner is formed on a transistor gate conductor and also as a liner between nitride spacers, to act as an etch stop so that the spacers can be formed and removed separately (col 8 ln 17-22). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Fulford on the device of Luning so that the nitride spacers could be formed and removed separately from the underlying oxides.

9. Regarding claims **30-34**, Luning discloses the structure of claims 1 and 8 with first and second nitride spacers. Fulford teaches that an oxide liner is formed on a transistor gate conductor and also as a liner between nitride spacers, to act as an etch stop so that the spacers can be formed and removed separately (col 8 ln 17-22). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Fulford on the device of Luning so that the nitride spacers could be formed and removed separately from the underlying oxides

***Response to Arguments***

10. Applicant's arguments with respect to claims 26-34 have been considered but are moot in view of the new ground(s) of rejection.

11. Applicant's arguments with respect to claims 1-2, 4-9 and 12-14 have been fully considered but they are not persuasive. These claims do not recite an oxide liner on the first and second gate conductors, wherein said first spacers are on the oxide layer.

***Conclusion***

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John C. Ingham whose telephone number is (571) 272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Howard Weiss/
Primary Examiner
Art Unit 2814

John C Ingham
Examiner
Art Unit 2814

/J. C. I./